



Fairness Control in WDM Slotted-Ring Networks

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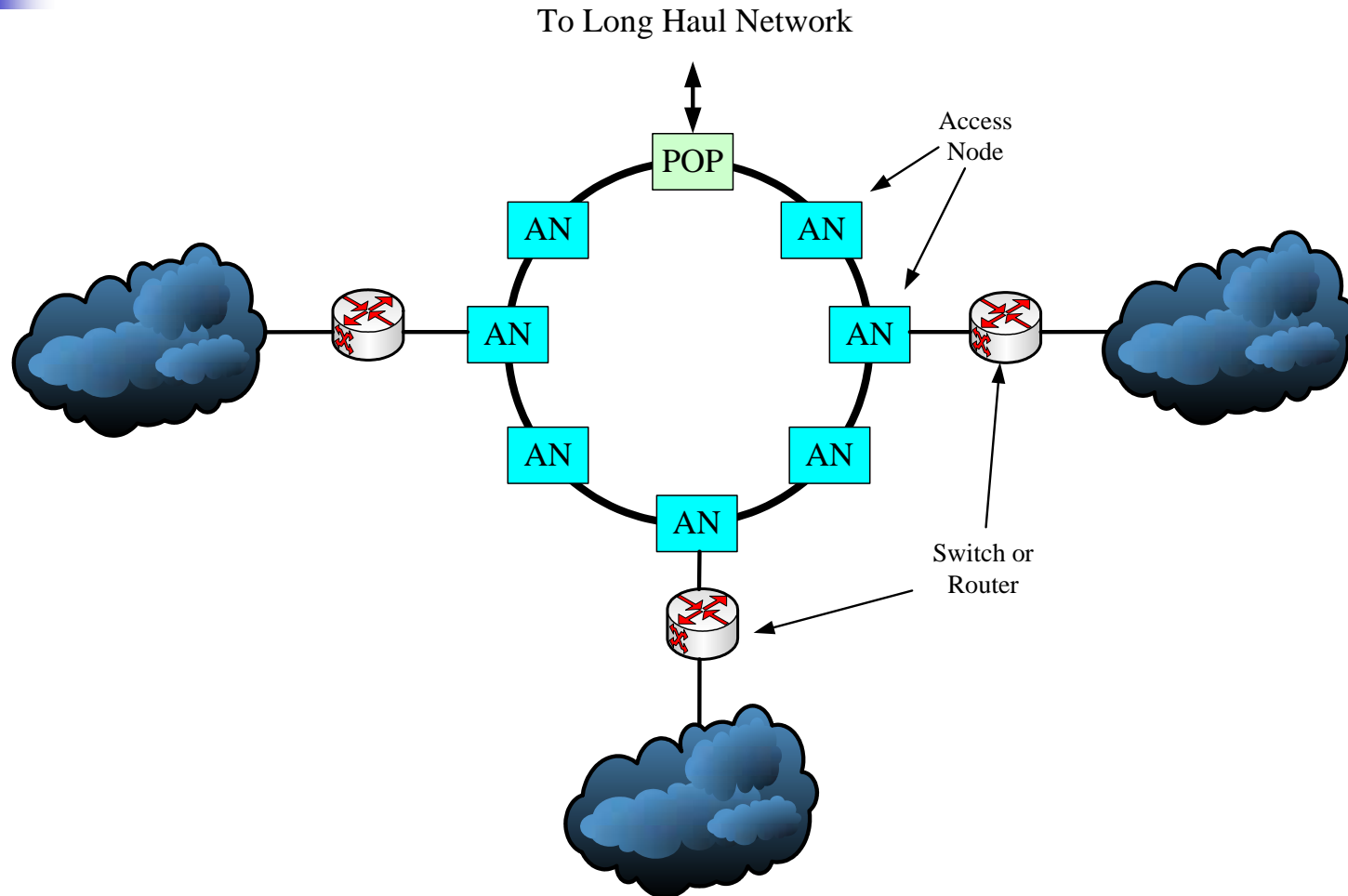
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Outline

- WDM Slotted-Ring Network Architecture
- MAC for WDM Slotted-Ring Networks
- Fairness Problems
- Multi-FECCA Fairness MAC Protocol
- RRC and RST Local Fairness Mechanisms
- Conclusion

WDM Ring Network Infrastructure





WDM Network Architecture

- Depending on the equipped transmitters and receivers on each node of the network
 - FT^N-FR^N: *N* Fixed Transmitters and *N* Fixed Receivers
 - TT-FR: *One* Tunable Transmitter and *One* Fixed Receiver
 - FT-TR: *One* Fixed Transmitter and *One* Tunable Receiver



MAC for WDM Slotted-Ring Networks

- To avoid collisions on the individual WDM channels, MAC protocols are necessary to arbitrate the bandwidth access.
- MAC design goals
 - Fairness
 - Bandwidth utilization
- Network architecture assumptions of WDM slotted-ring MAC protocols
 - Wavelengths = Nodes: each node is associated with a particular wavelength
 - Wavelengths < Nodes: multiple nodes share a single wavelength



Data Removal Mechanisms

- Source stripping

- Source node is responsible for removing the data from the ring.

- Lower bandwidth utilization: $\rho_s = \frac{N}{N+1}$

- Destination stripping

- Destination node is responsible for removing the data from the ring.

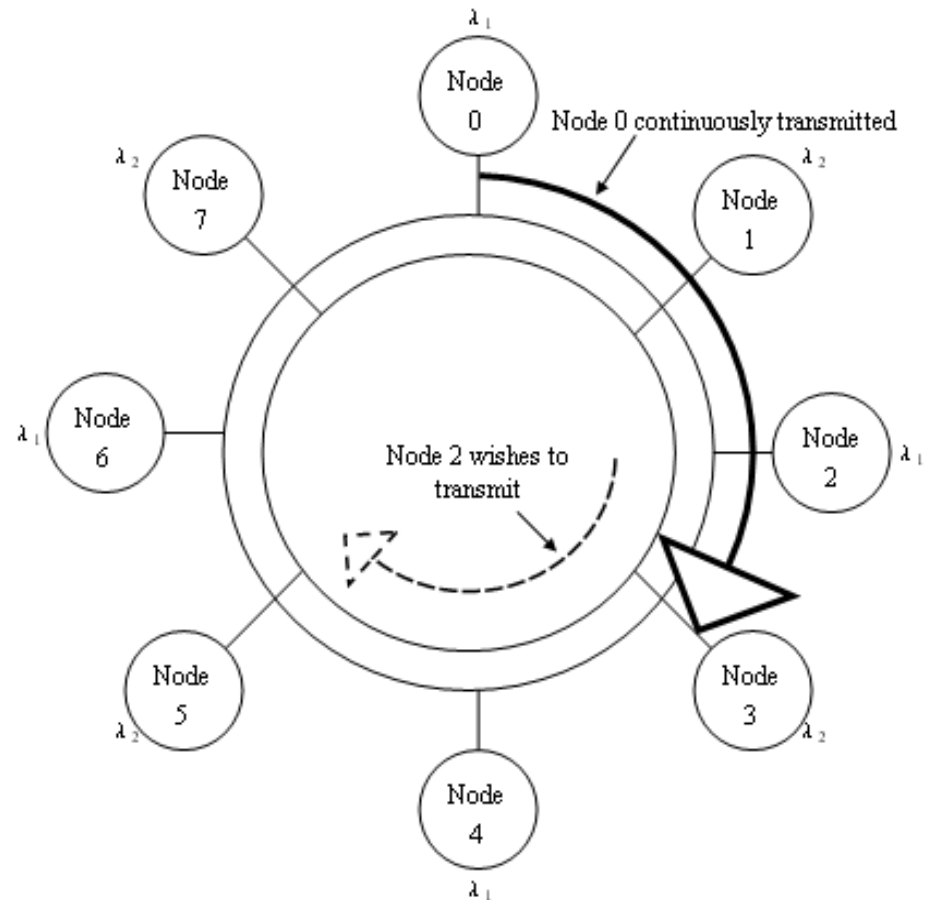
- Allow spatial reuse

- Better bandwidth utilization: $\rho_d = \frac{2N}{2+N}$

N : the number of nodes on the ring.

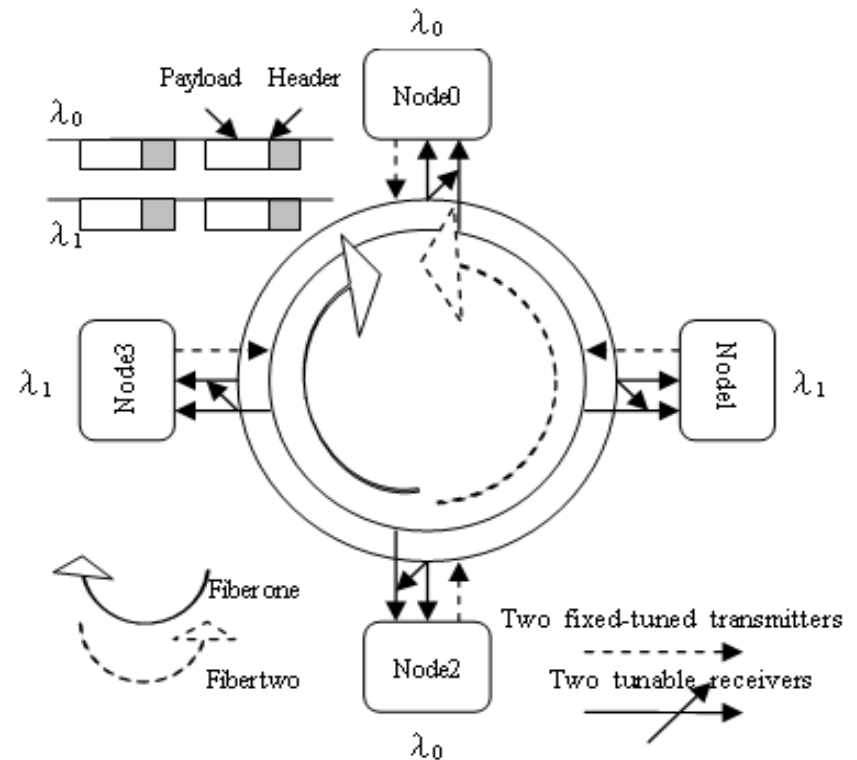
Why “Unfairness” Occurs?

- Fairness problems may occur, especially under unbalanced traffic pattern
 - A heavy traffic node may continuously seize the bandwidth for a long time.
 - Downstream nodes may suffer starvation



Target WDM Slotted Ring

- A full-duplex WDM slotted ring
 - Dual fiber rings:
 - Clockwise: Ring A
 - Counter-Clockwise: Ring B
 - More nodes than the available wavelengths
 - Each wavelength has some fixed-length slots rotating around the ring
 - Time slots are completely synchronized between wavelengths
- Each node is equipped with one Fixed-tuned Transmitter (FT) and one Tunable Receiver (TR) on both rings
 - Each node is allowed to transmit only on the assigned wavelength but can receive on any wavelengths





ATMR Control Mechanism¹

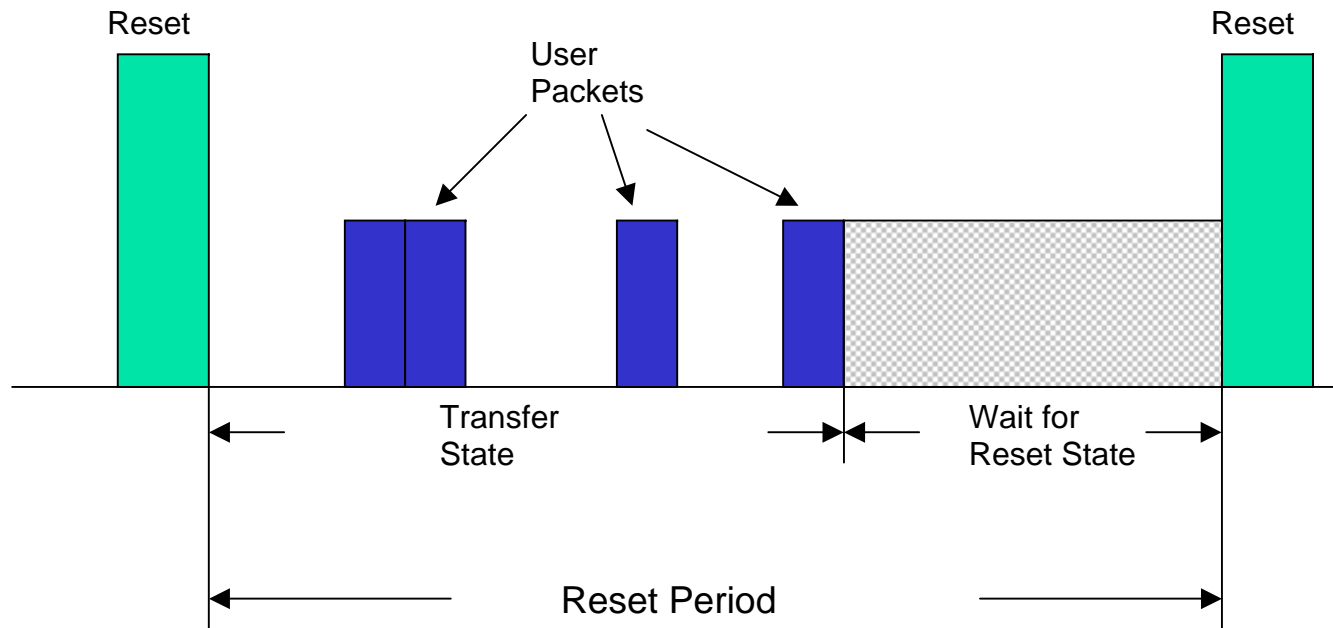
- A cycle-based control scheme
 - Originally designed for ATM ring network
 - Each node has a transmission quota, *Wins*, within each fairness cycle
 - Each slot consists of two segments
 - Header
 - Payload
 - The busy address field in the header serves as the control message which rotates at the same direction of the user data.



ATMR Control Mechanism²

- Each node can be in one of the following two states
 - Active state
 - Not yet used up its transmission quota and has packets stored in the queue
 - Waits for an empty slot to transmit
 - Write its own address in the busy address field of every incoming slot
 - Become an inactive node when completely exhausts its transmission quota or has no packets in the queue
 - Inactive state
 - Used up its transmission quota or has no packets stored in the queue
 - Stops writing its own address in the busy address field
 - Upon discovering its own address in the busy address field of a slot, it knows that all nodes have completed their transmissions.
 - Issues a reset signal to start a new cycle.
 - Upon receiving the reset signal, each node sets its transmission quota back to the default value.

ATMR Reset Mechanism



- Inactive nodes can not send until next reset even if their transmissions do not affect the fairness.
- Wasted bandwidth



M-ATMR Access Algorithm

- Bengi and *et al*/ have applied ATMR scheme on each wavelength of an unidirectional TT-FR system, referred to as M-ATMR mechanism.
- However, M-ATMR mechanism suffers the same bandwidth utilization problem as in ATMR on each wavelength.

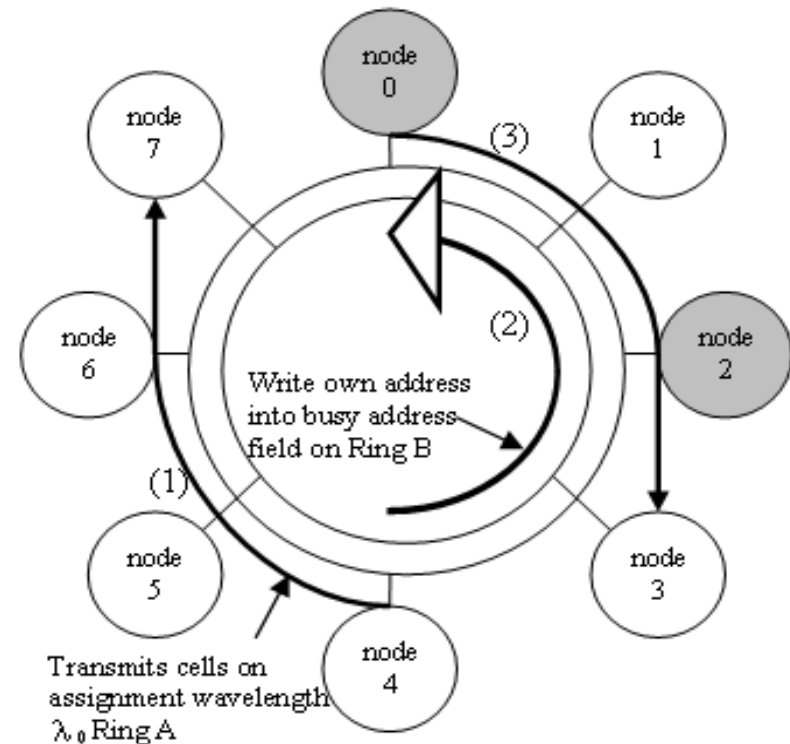


Multi-FECCA Access Algorithm¹

- Based on the extension of M-ATMR for full-duplex FT-TR systems
 - Cycle-based control scheme
 - Busy address fields are used as control messages
 - Data and control messages are sent in opposite directions
 - When data are transmitted on Ring A, their control messages are sent on Ring B and vice versa
- Each wavelength of both Ring A and Ring B employs Multi-FECCA access algorithm independently

Multi-FECCA Access Algorithm²

- When a new fairness cycle starts, each active node writes its own address in the busy address field of each incoming slot on Ring B
- By monitoring the busy address field of an incoming slot on Ring B, each upstream node on Ring A will know who is its nearest downstream active node.
- Combined with destination removal technique and spatial reuse, inactive nodes may gain additional transmission opportunities without affecting the transmissions of active nodes.





Simulation Assumptions

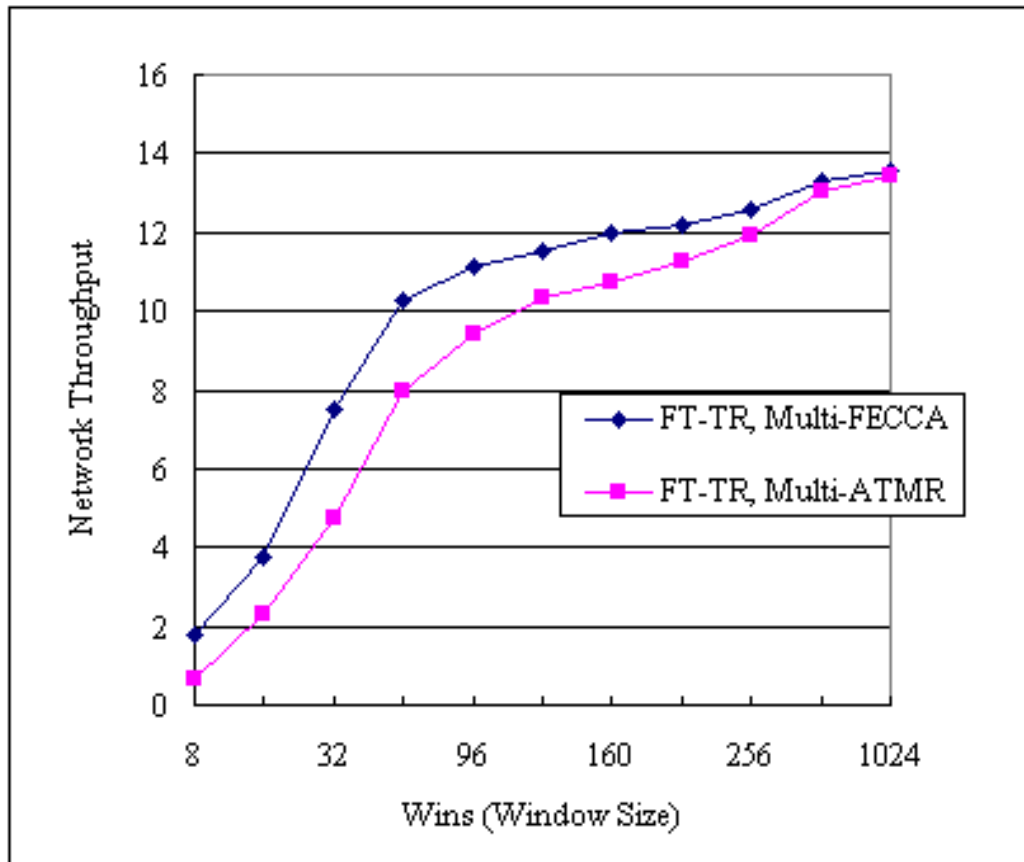
- FT-TR system has 64 nodes
- Each ring has 4 wavelengths $\{ \lambda_0, \lambda_1, \lambda_2, \lambda_3 \}$ and each wavelength has 256 time slots.
- Unbalanced traffic load conditions
 - Nodes 8, 9, 10, 11, 17, 28, 29, 32, 36, 41, 42 and 52 are assumed to be fully loaded.
 - 50% of traffic on Node 9 is destined to node 15.
 - All other nodes are lightly loaded based on a Poisson process at a rate 0.05 [cells / slot] with their destinations being uniformly distributed.



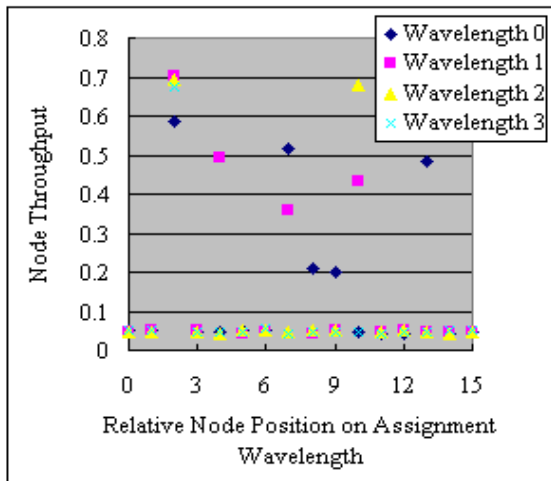
Relative Node Position

Relative node position Assigned channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Channel 0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60
Channel 1	1	6	9	13	17	21	25	29	33	37	41	45	49	53	57	61
Channel 2	2	5	10	14	18	22	26	30	34	38	42	46	50	54	58	62
Channel 3	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63

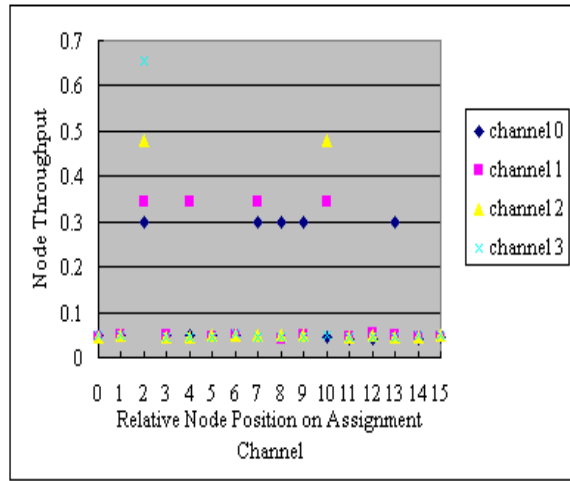
Throughput vs *Wins*



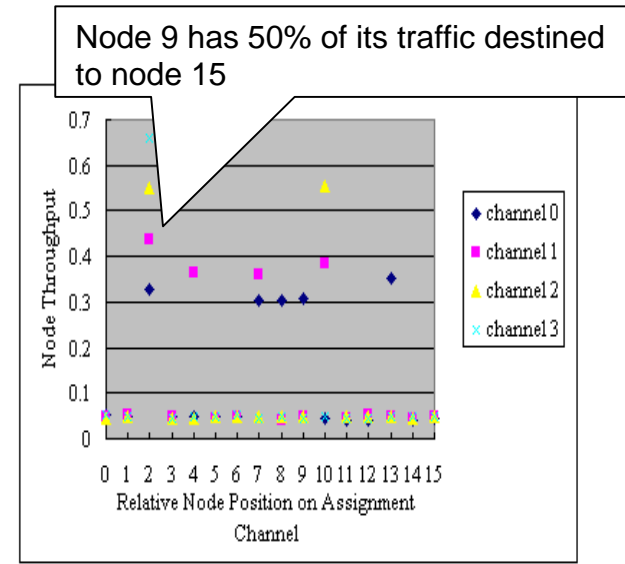
Throughput Comparison



(a)



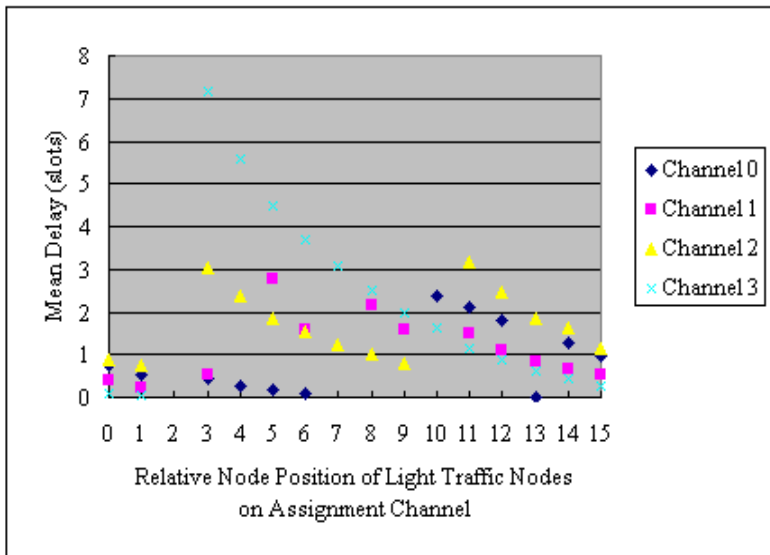
(b)



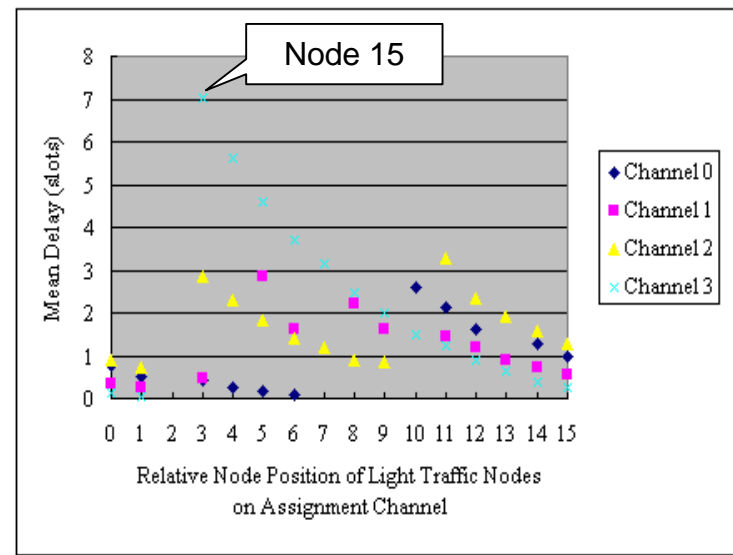
(c)

(a) Destination-stripping (b) Multi-ATMR (c) Multi-
FECCA

Mean delay



(a)



(b)

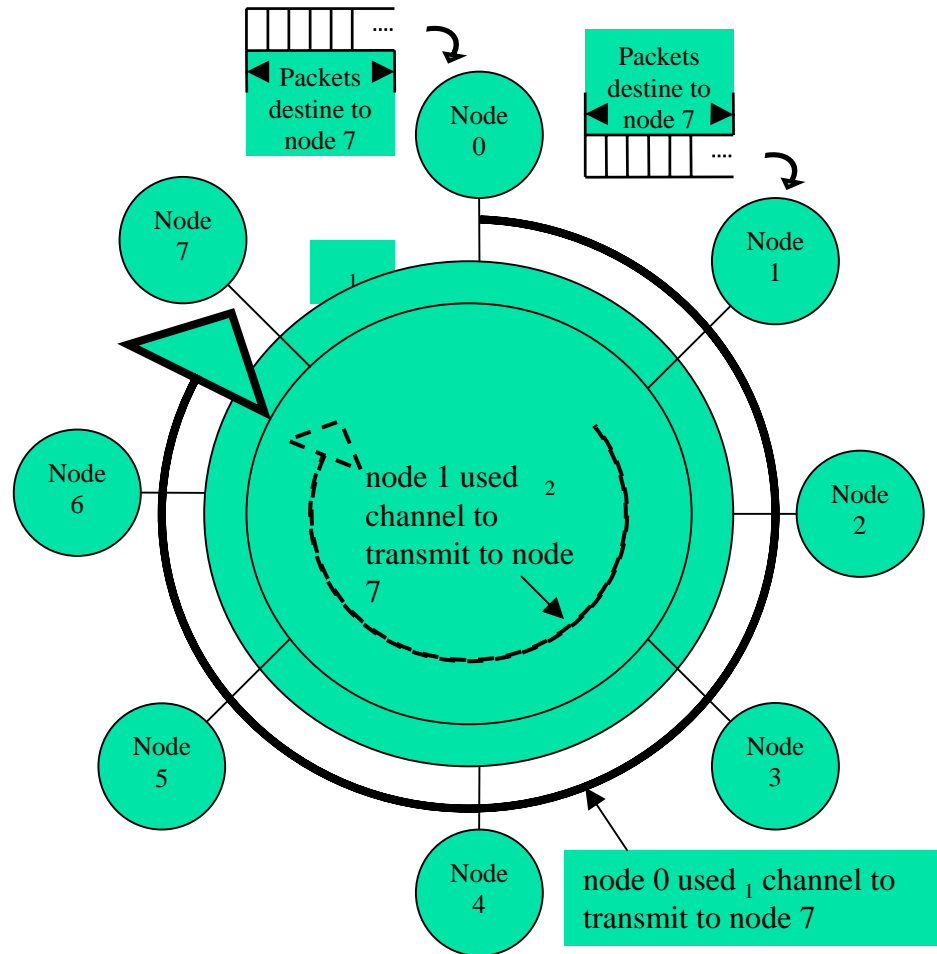
Mean delay of light traffic nodes (a) M-ATMR (b) M-FECCA



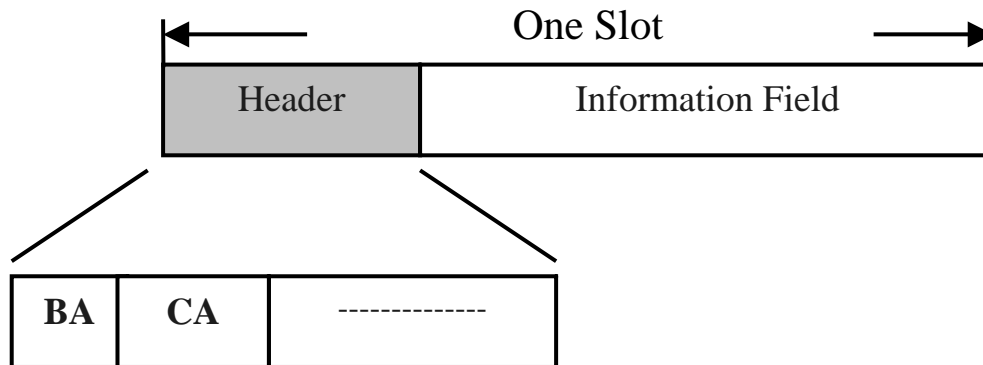
Receiver Collision

- Receiver collision: When multiple packets destined to the same destination arrive at the same time slot in FT-TR systems.
- A straight forward way to resolve receiver collision is to have the destination pick one packet and let all other packets loop around the ring.
- If each node guarantees that no two packets at any time slot across all wavelengths destined to the same destination, then receiver collision is solved.
- But this causes a new fairness problem, referred to as local fairness problem, among nodes at different wavelengths all sending to the same destination.

Local Fairness Problem



Slot Format



BA: Busy Address, this field indicates the active node address.

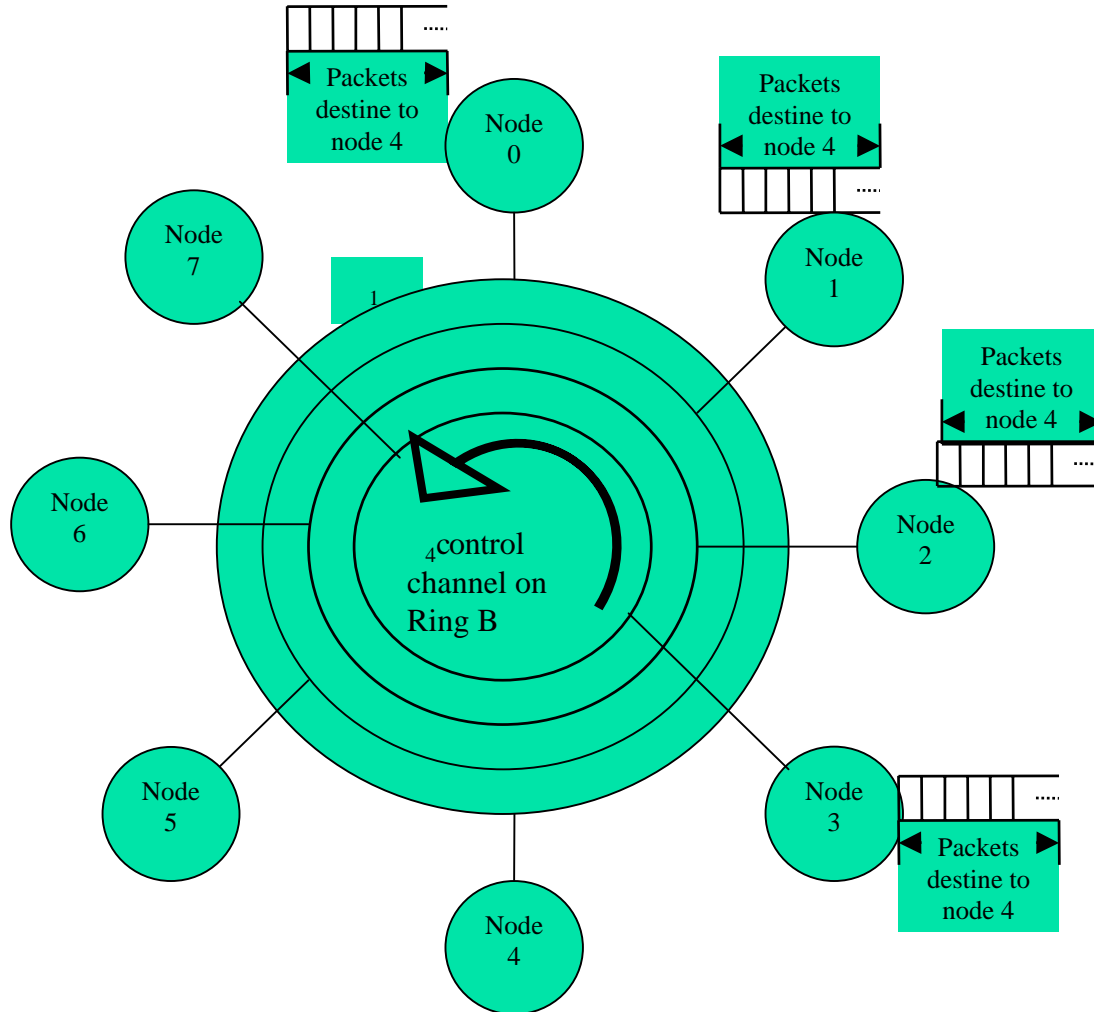
CA: Collision Address + Congested node address



Round Robin Control (RRC)

- Each node can tolerate contiguous transmission delay Q_d .
- When transmission delay $D \geq Q_d$
 - Write the node address and collision destination node address into collision address field (CA)
 - Set $D = 0$
- Whenever upstream nodes detect CA field is not empty, they will not send data to the heavy sink destination for a few slots, depending on the number of downstream congested nodes.
- All nodes sending to the heavy sink destination will take turns in round-robin fashion eventually.

RRC Access Control

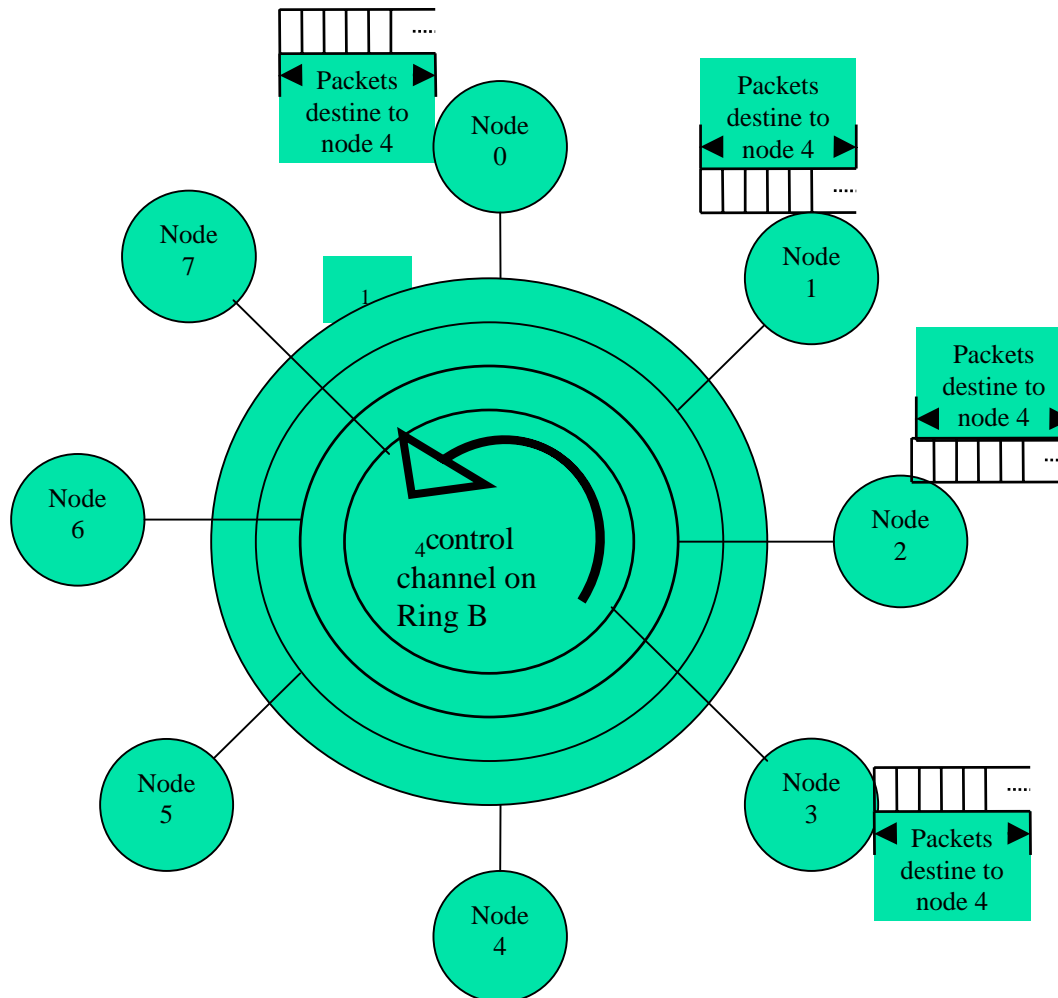


Reserve Slot for Transmission (RST)



- Each node is allowed to tolerate contiguous transmission delay quota Q_d .
- Transmission delay $D = Q_d$
 - Reserve the empty slot by writing its own address into the collision address field (CA)
- Whenever upstream nodes detect CA field is not empty
 - Release the empty slot for the downstream nodes
- The downstream node will set D back to zero after writing its own address into CA.

RST Access Control

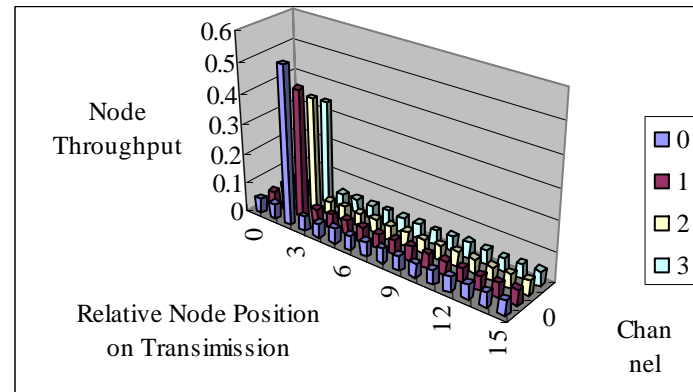
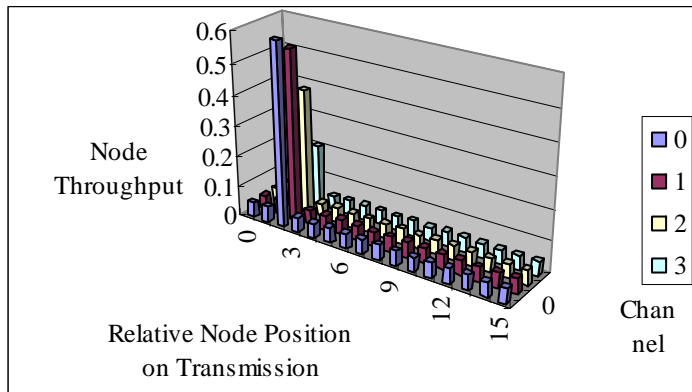




Simulation Assumptions

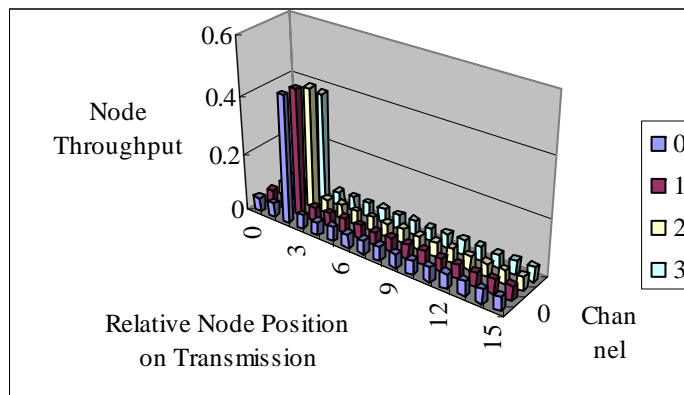
- Same as the previous simulation setup
- Unbalanced traffic load
 - Nodes 8~11 have traffic load = 0.7 packets/slot and 50% data destined for node 24
 - All other nodes have traffic load = 0.05 packets/slot with destination being uniformly distributed
- For both RRC and RST simulations, Q_d is set to 2.

Throughput



(a)

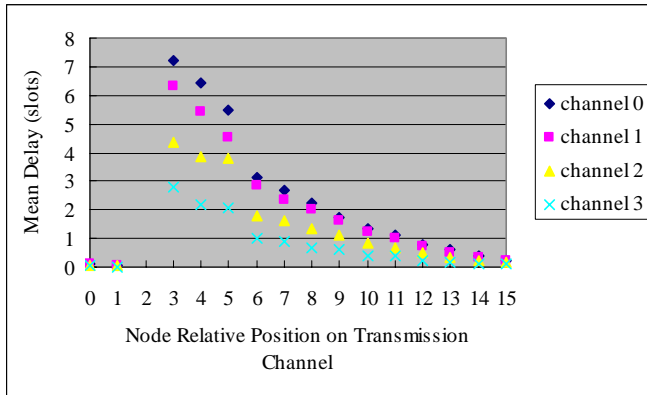
(b)



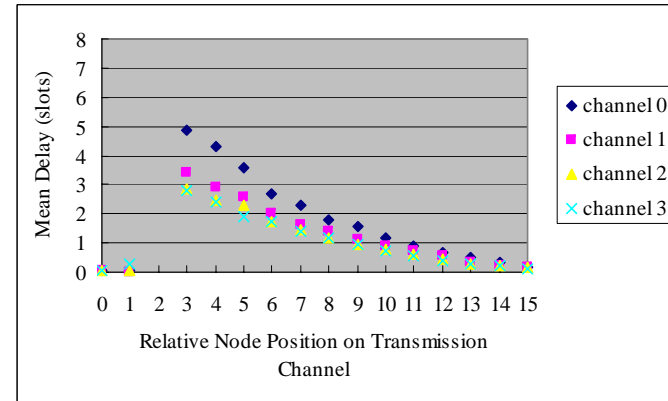
(c)

Fig. (a) Multi-FECCA. (b) Multi-FECCA with RST. (c) Multi-FECCA with RRC.

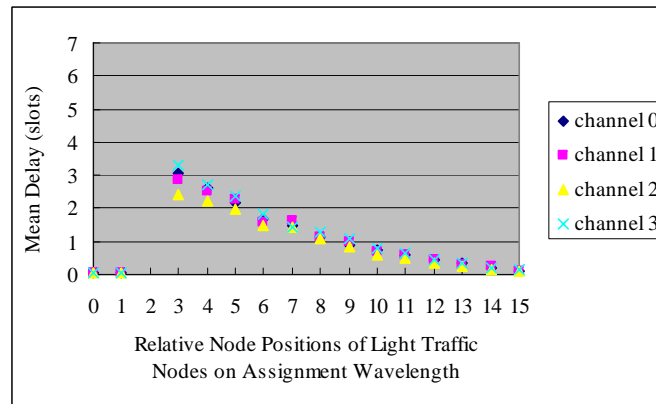
Delay



(a)



(b)



(c)

Fig. (a) Multi-FECCA. (b) Multi-FECCA with RST. (c) Multi-FECCA with RRC.



Conclusion

- Propose Multi-FECCA MAC protocol for full-duplex FT-TR WDM slotted-ring networks.
- Multi-FECCA
 - Provide excellent fairness guarantee
 - Achieve better throughput without compromising fairness guarantee
- Propose RRC and RST for resolving local fairness problem under unbalanced traffic load and heavy sink conditions